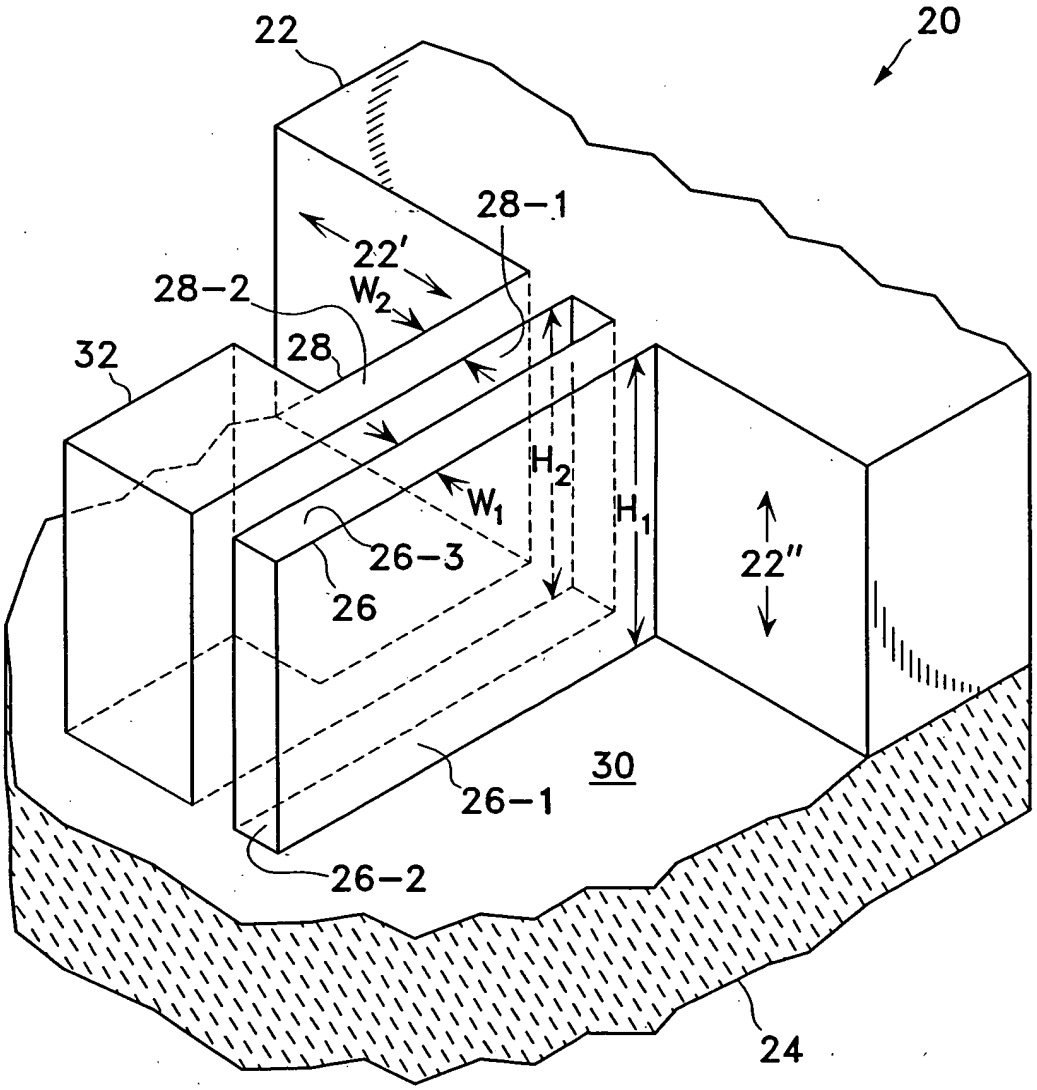


Fig. 1

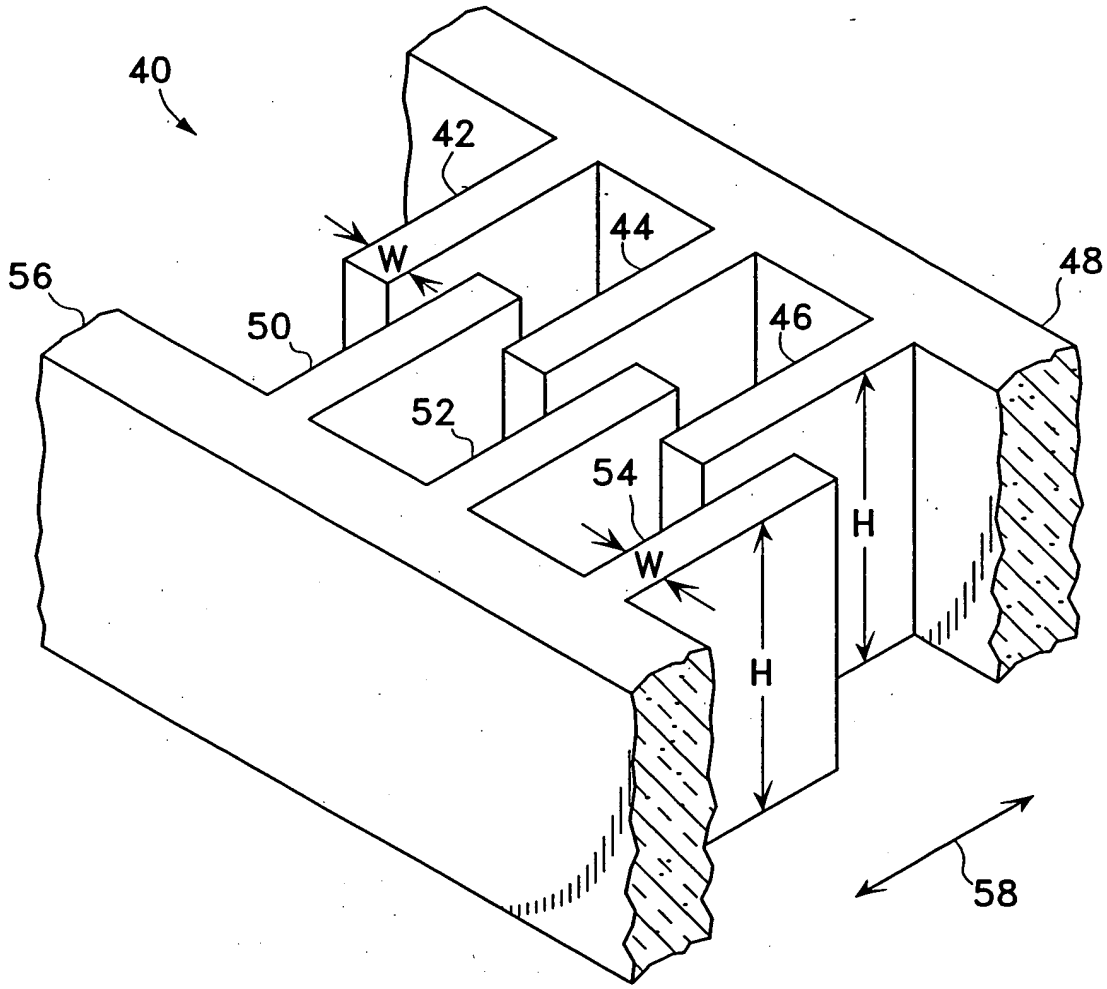


Fig. 2

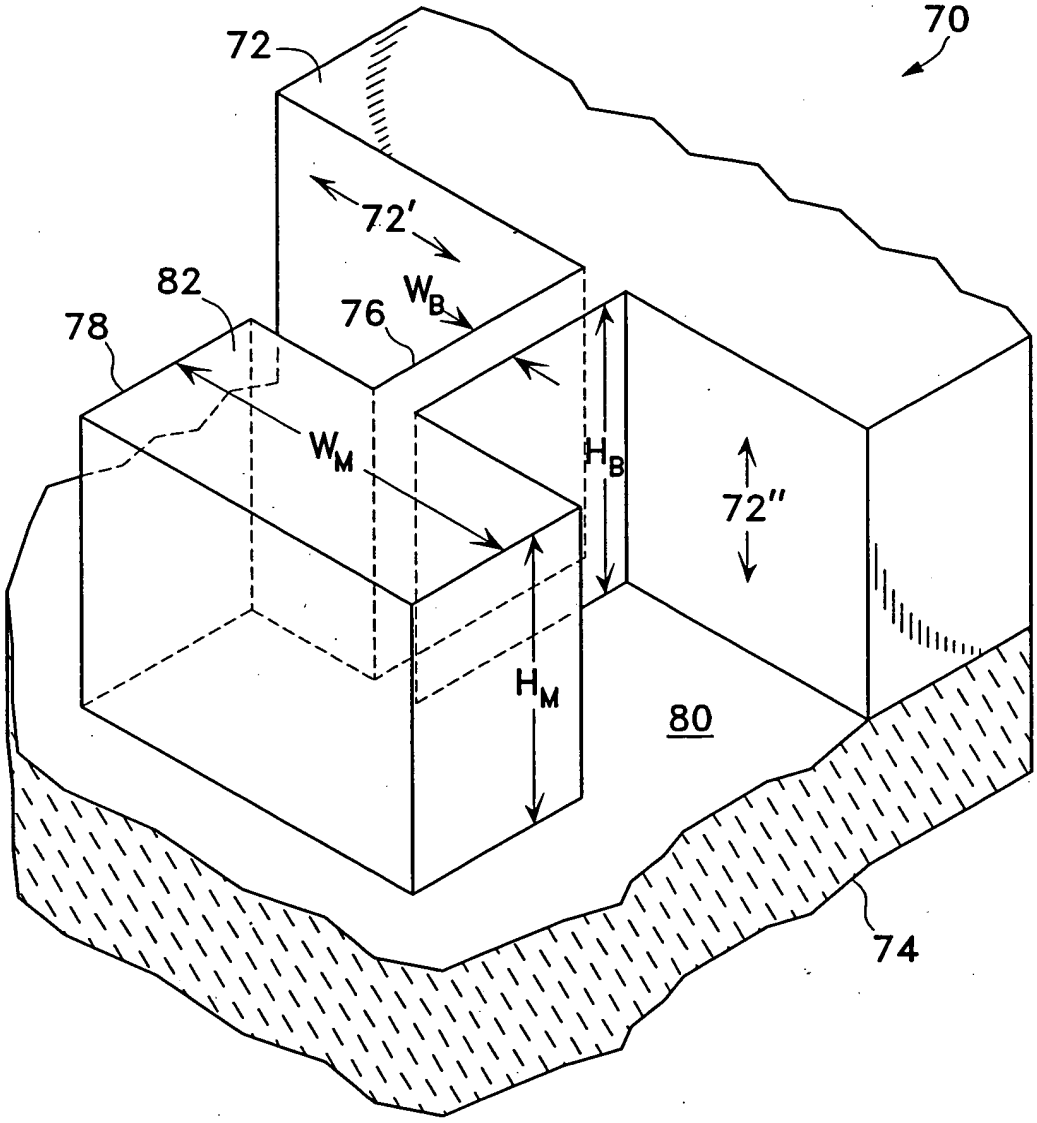


Fig. 3

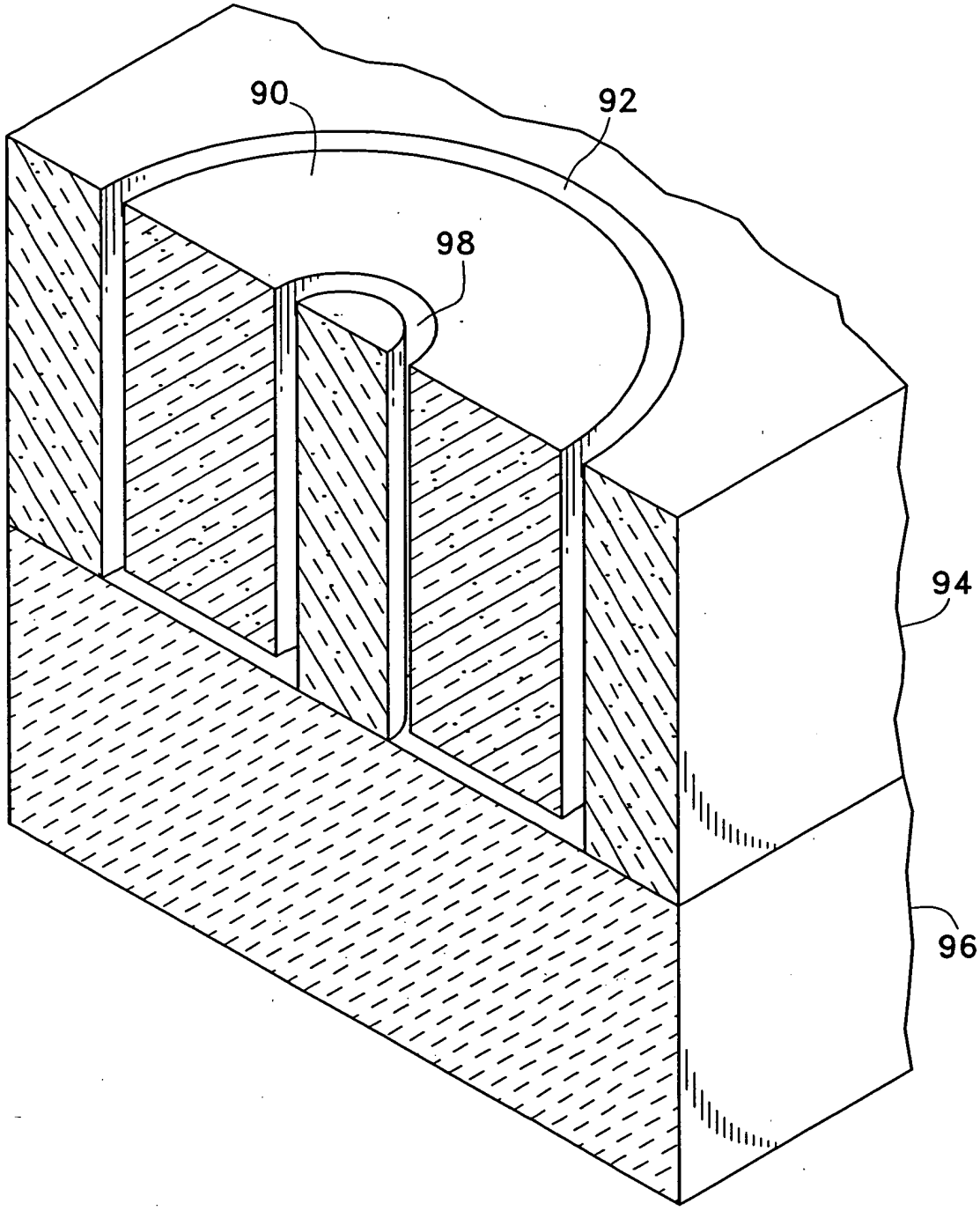


Fig. 4

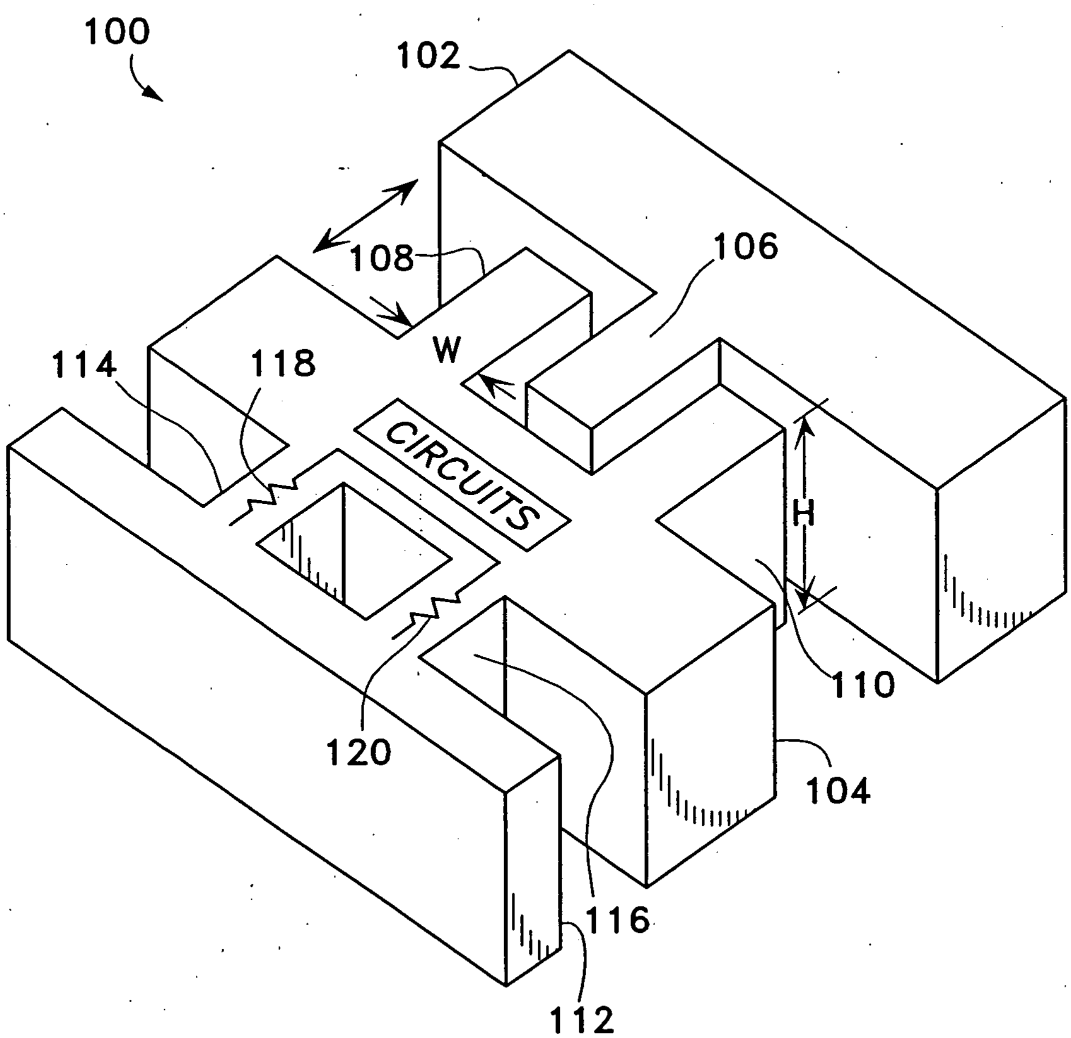


Fig. 5

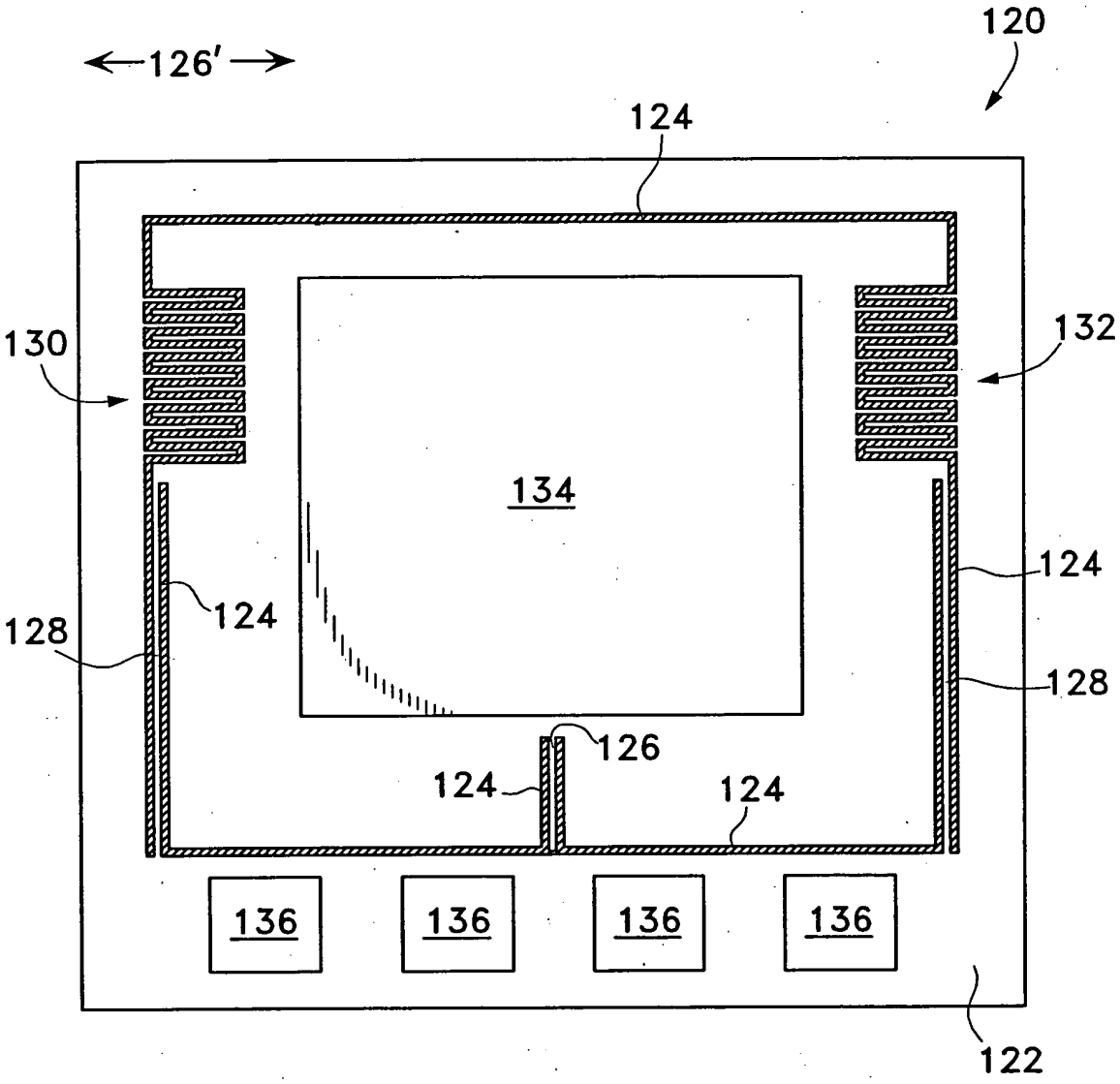

120
126'
124
130
132
134
124
124
128
128
126
124
124
136
136
136
136
122

Fig. 6

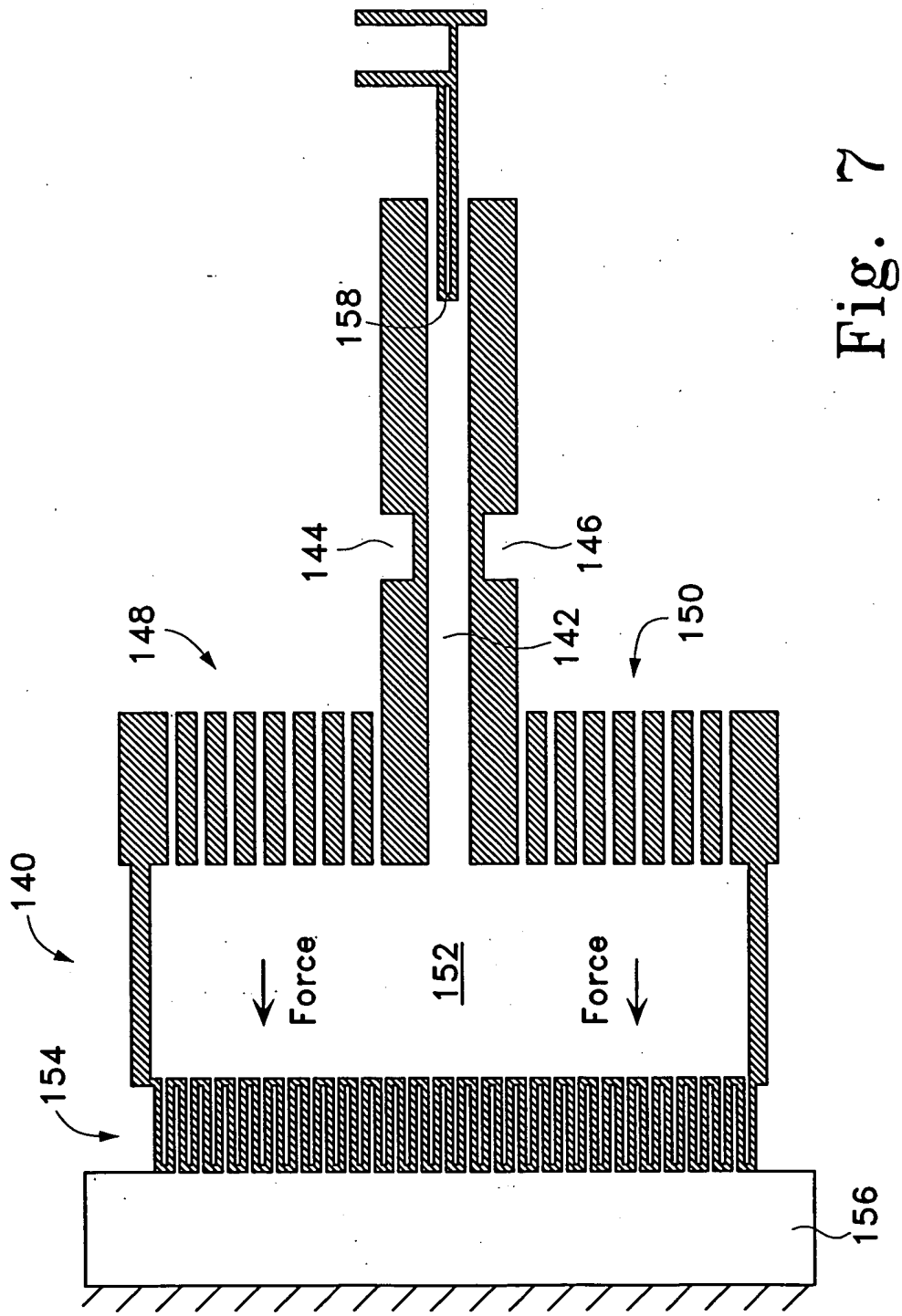


Fig. 7

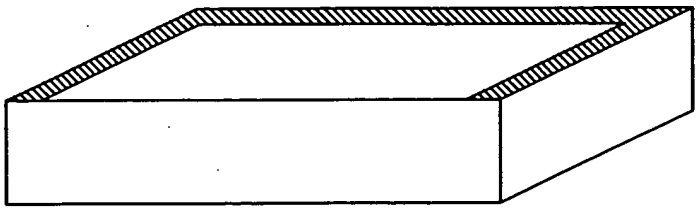


Fig. 8A

Pattern frontside with cavity mask and backside with alignment markers.

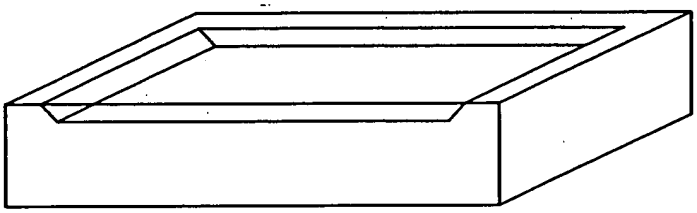


Fig. 8B

Timed anisotropic or plasma etch to form cavities.
Strip frontside insulator.

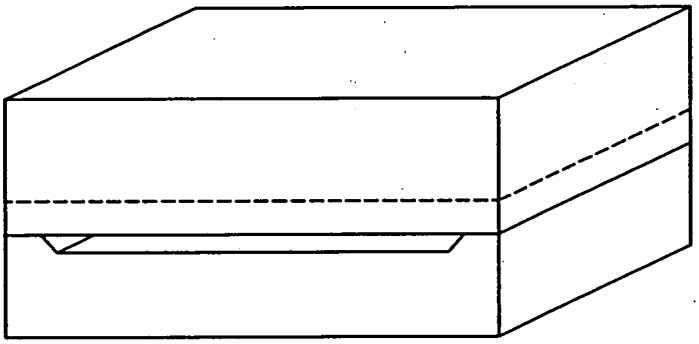


Fig. 8C

Silicon fusion band epi wafer to frontside. Epi thickness determines MEMS device thickness.

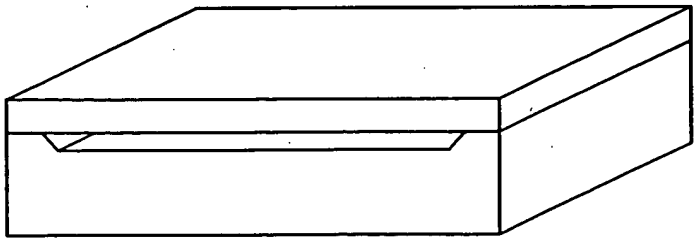
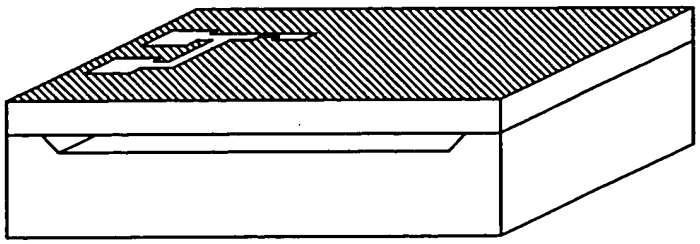


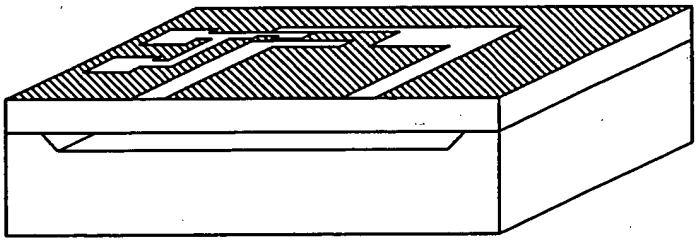
Fig. 8D

ECE etch to epi interface.



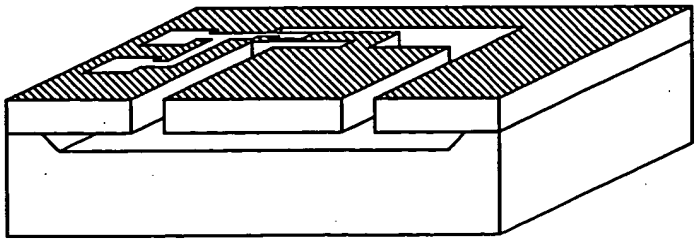
Deposit insulator on frontside and process sensing on chip circuits.

Fig. 8E



Define MEMS structure in insulator layer.

Fig. 8F



Anisotropic plasma etch to form MEMS structure.

Fig. 8G

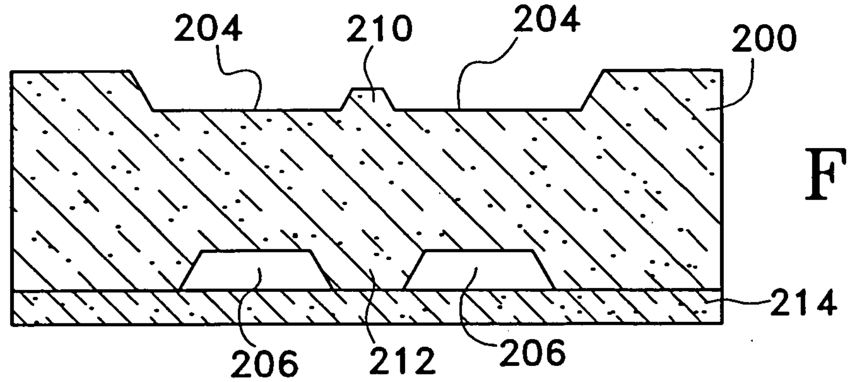


Fig. 9A

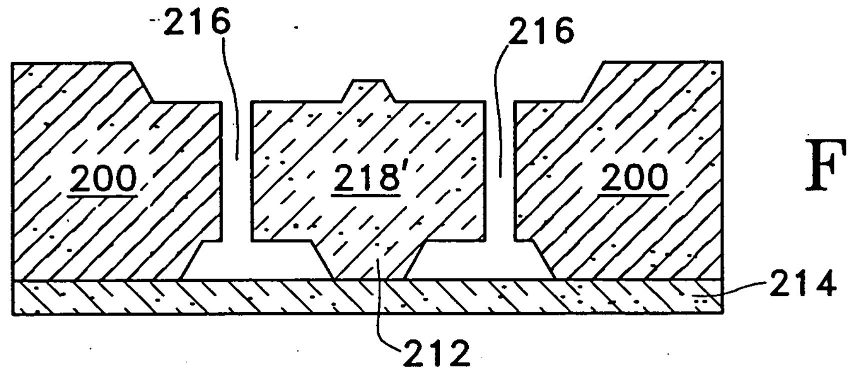


Fig. 9B

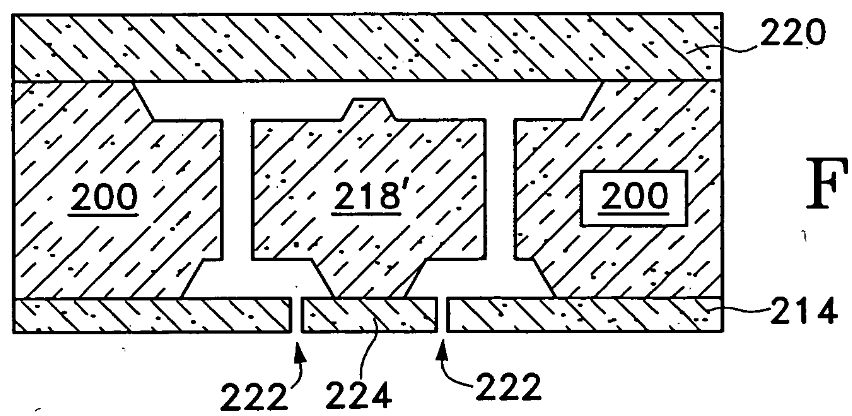


Fig. 9C

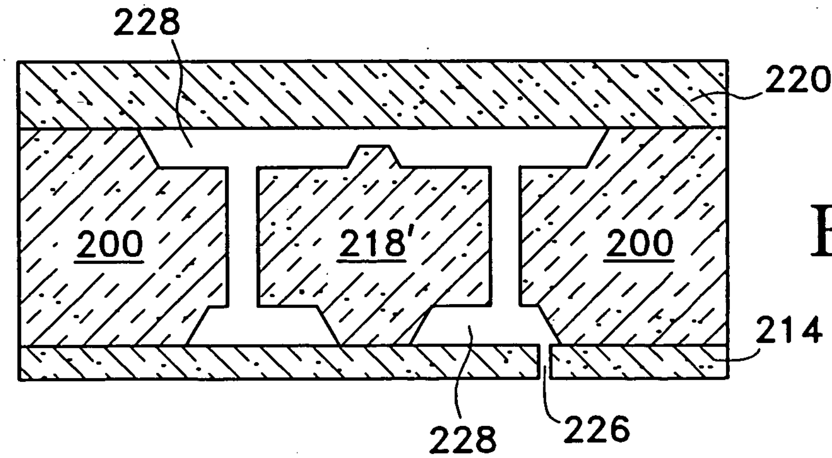


Fig. 9D

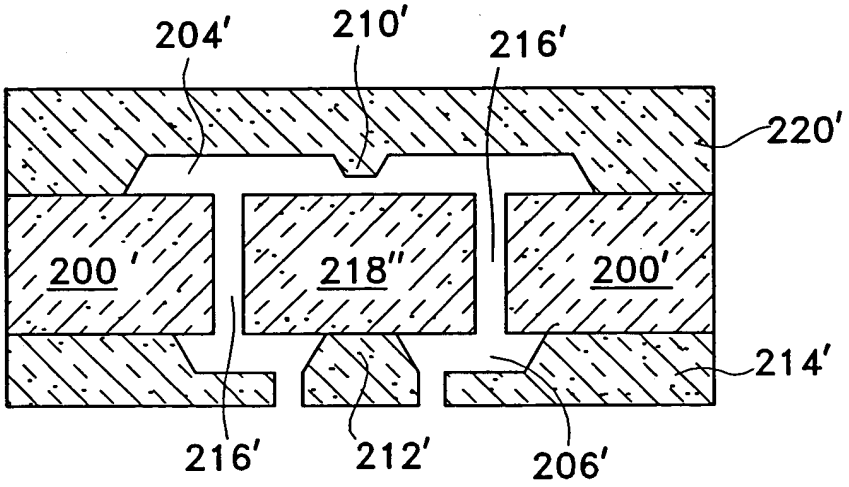

204'
210'
216'
220'
200'
218''
200'
214'
216'
212'
206'

Fig. 10

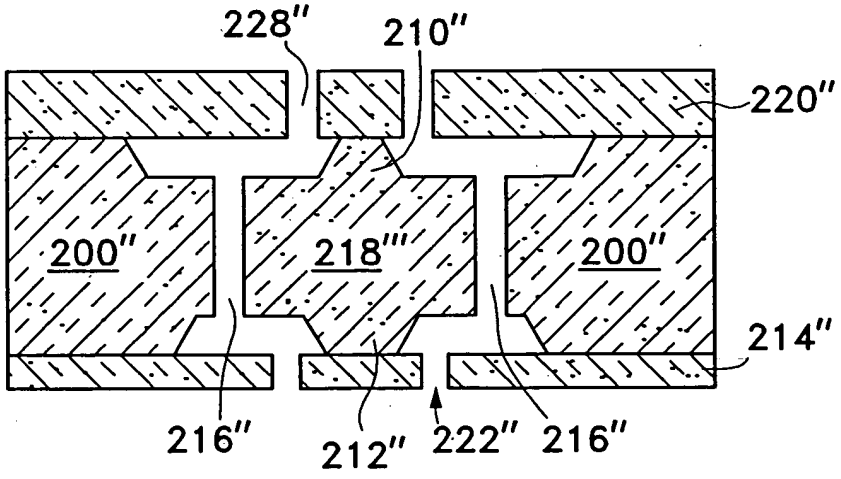

228''
210''
220''
200''
218'''
200''
214''
216''
212''
222''
216''

Fig. 11

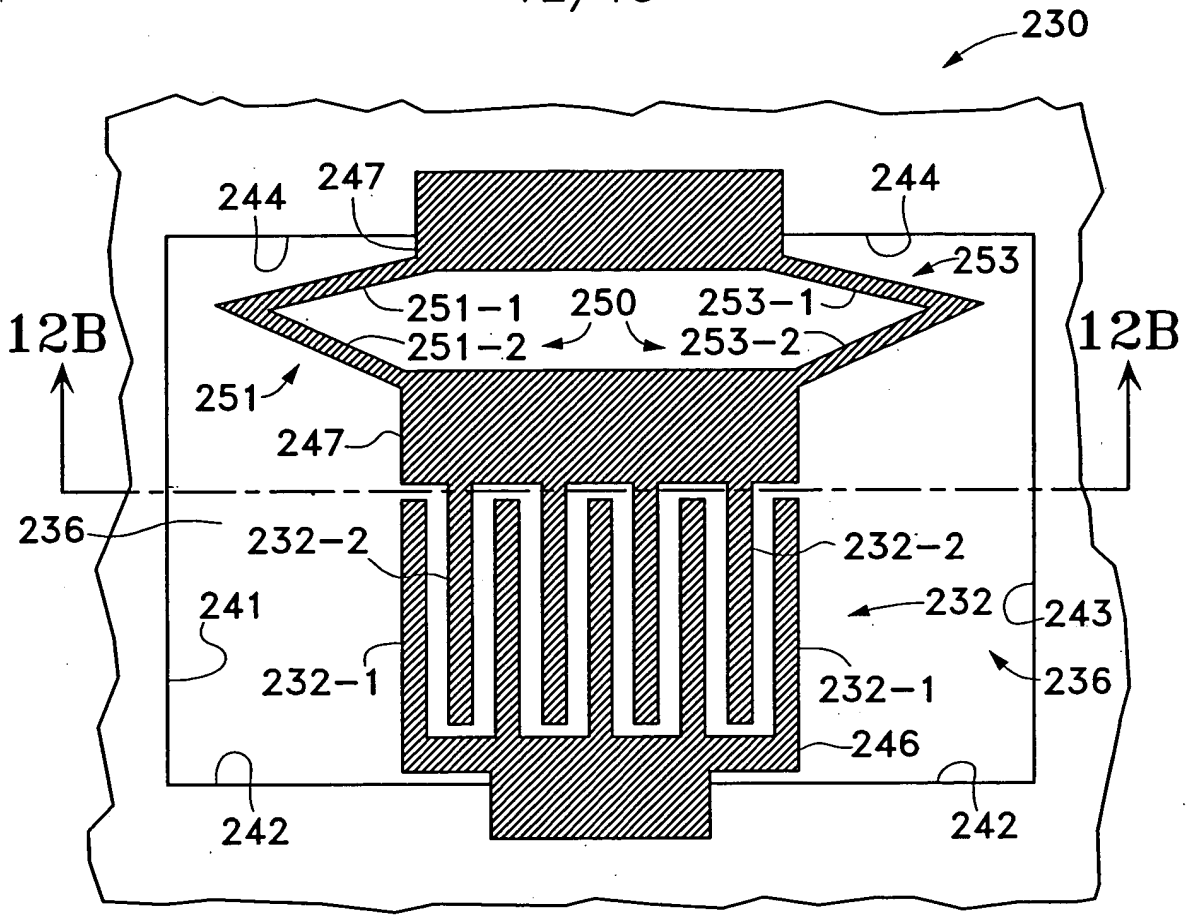


Fig. 12A

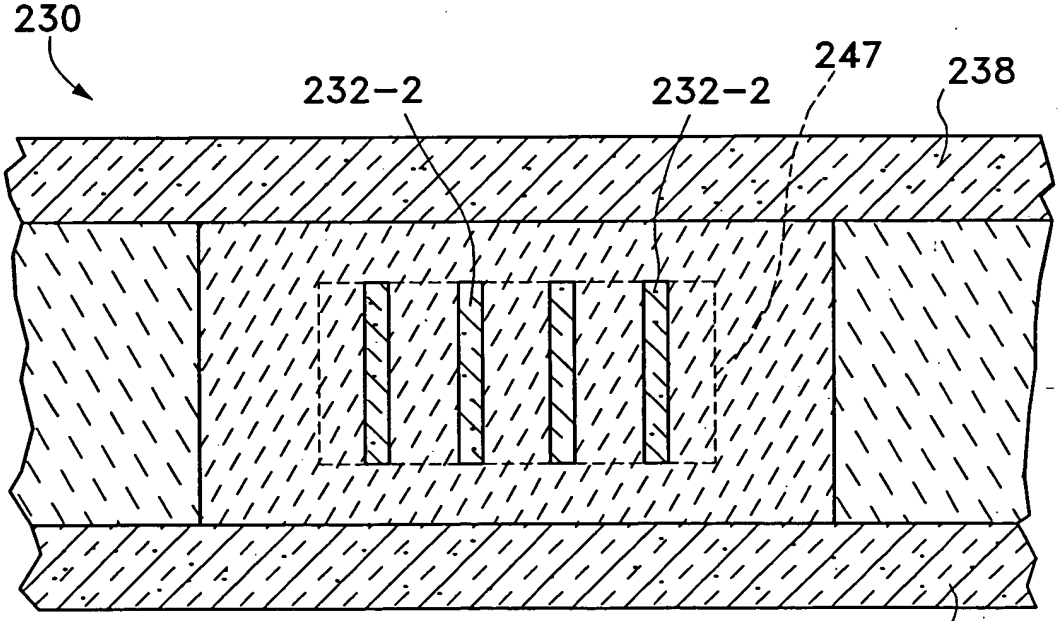


Fig. 12B

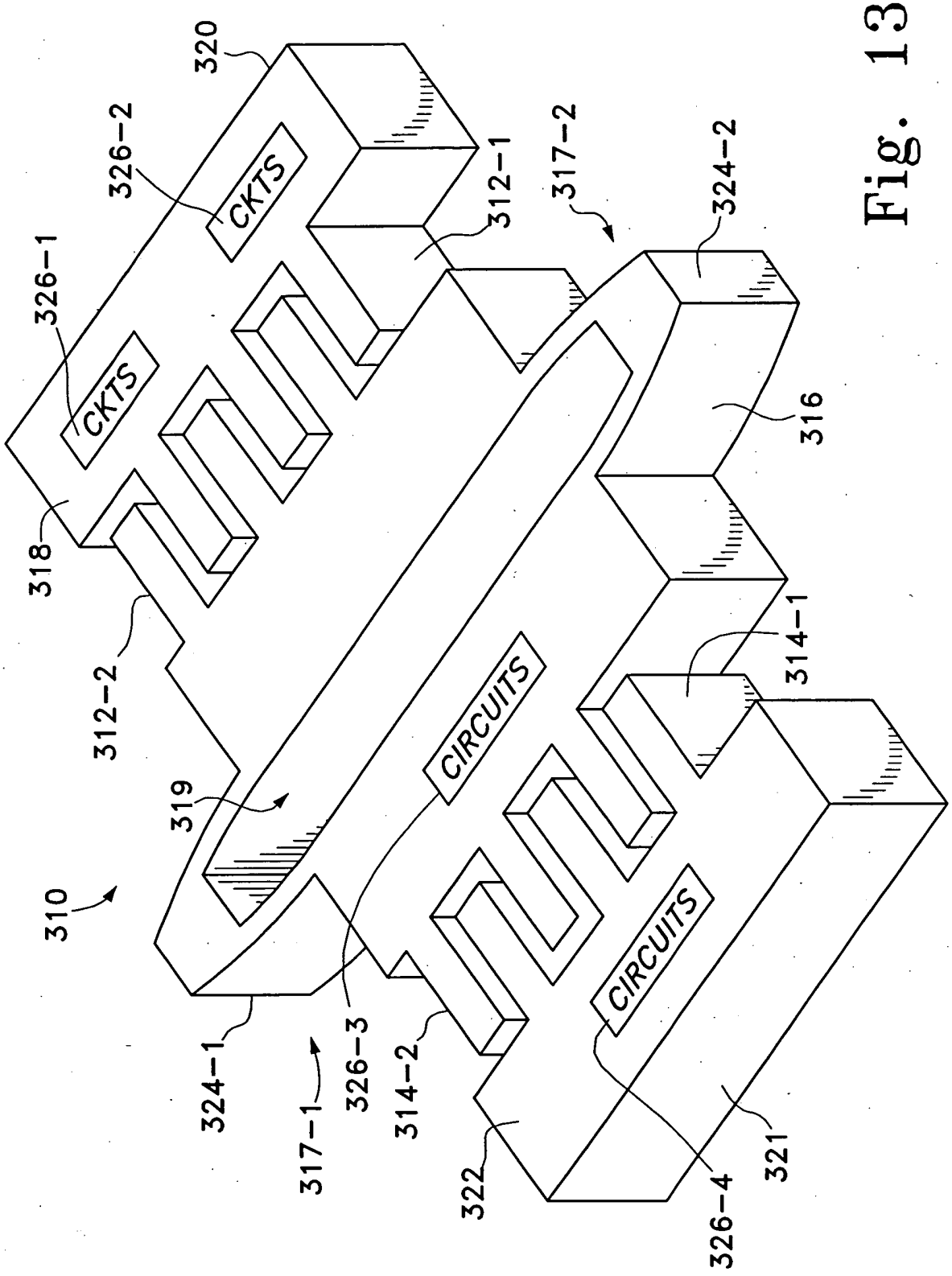

320
326-2
CKTS
326-1
CKTS
312-1
317-2
324-2
316
318
312-2
314-1
319
CIRCUITS
310
CIRCUITS
324-1
326-3
314-2
317-1
322
326-4
321

Fig. 13